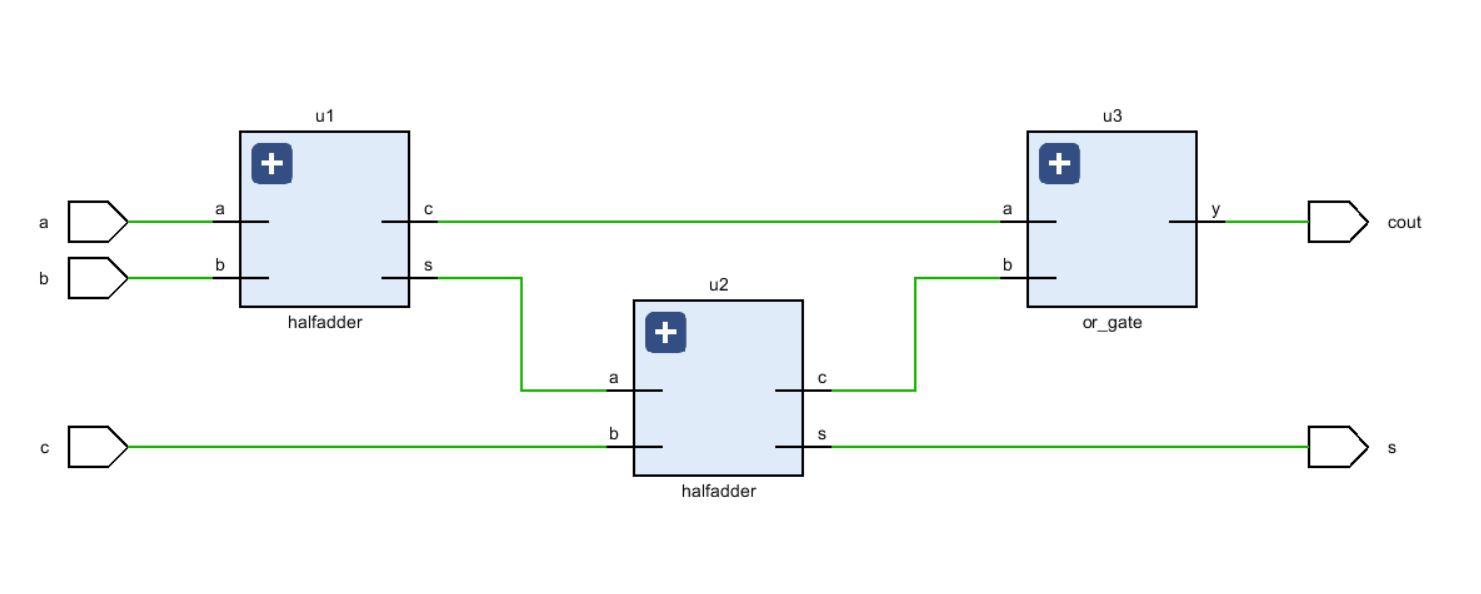
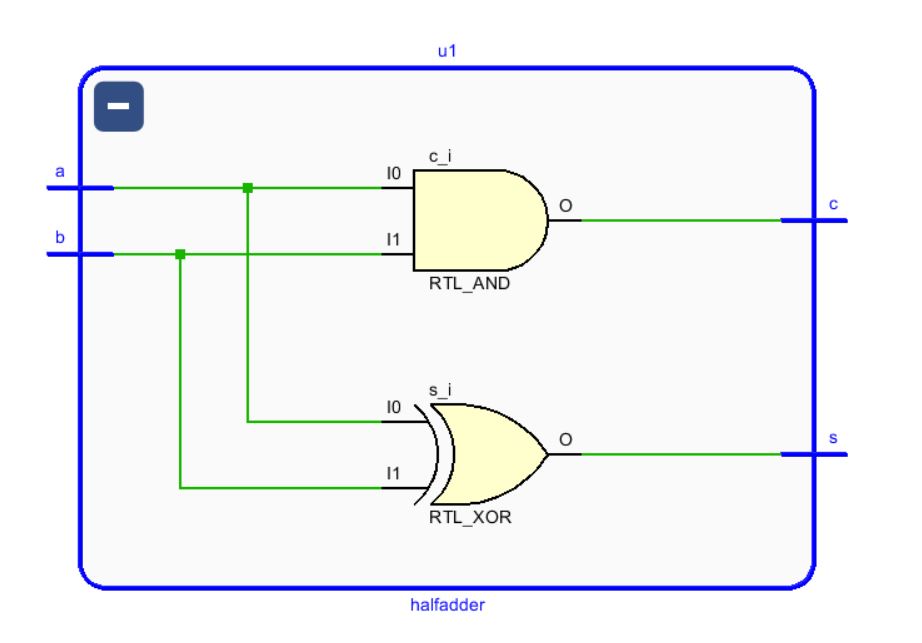
**Practical 3**

**Aim:** Write a VHDL Code to implement Half Adder. Also write VHDL code for Full Adder with the instance of implemented Half adder

|  |
| --- |
| **Code:**  library IEEE;  use IEEE.STD\_LOGIC\_1164.ALL;  entity fulladder is  Port ( a : in STD\_LOGIC;  b : in STD\_LOGIC;  c : in STD\_LOGIC;  s : out STD\_LOGIC;  cout : out STD\_LOGIC);  end fulladder;  architecture Behavioral of fulladder is  component halfadder is  Port ( a : in STD\_LOGIC;  b : in STD\_LOGIC;  s : out STD\_LOGIC;  c : out STD\_LOGIC);  end component halfadder;  component or\_gate is  Port ( a : in STD\_LOGIC;  b : in STD\_LOGIC;  y : out STD\_LOGIC);  end component or\_gate;  signal x,c1,c2:std\_logic;  begin  u1:halfadder port map(a,b,x,c1);  u2:halfadder port map(x,c,s,c2);  u3:or\_gate port map(c1,c2,cout);  end Behavioral; |

**RTL DIAGRAM:**

****

**Test bench Code :**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity Tb\_fulladder is

-- Port ( );

end Tb\_fulladder;

architecture Behavioral of Tb\_fulladder is

component fulladder is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

c : in STD\_LOGIC;

s : out STD\_LOGIC;

cout : out STD\_LOGIC);

end component fulladder;

signal a,b,c,s,cout:std\_logic;

begin

u1:fulladder port map(a,b,c,s,cout);

process

begin

a<='0';

b<='0';

c<='0';

wait for 10ns;

a<='0';

b<='0';

c<='0';

wait for 10ns;

a<='0';

b<='1';

c<='0';

wait for 10ns;

a<='1';

b<='1';

c<='0';

wait for 10ns;

a<='0';

b<='0';

c<='1';

wait for 10ns;

a<='0';

b<='0';

c<='1';

wait for 10ns;

a<='0';

b<='1';

c<='1';

wait for 10ns;

a<='1';

b<='1';

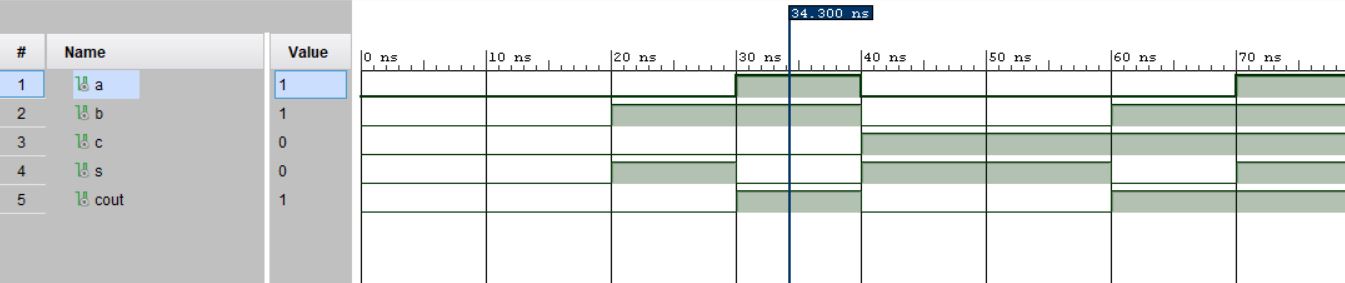
c<='1';

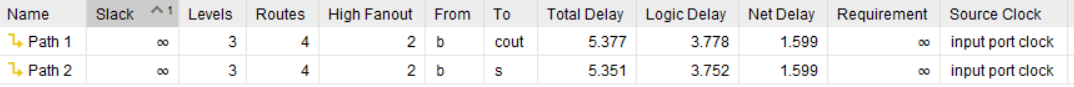
wait;

end process;

end Behavioral;

**SIMULATION WAVEFORM :**

****



**SYNTHESIS SUMMARY:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Resource** | **Utilization** | **Available** | **Utilization %** |
| LUT | 1 | 17600 | 0.01 |
| IO | 5 | 100 | 5.00 |

Maximum Combinational Delay: 5.377nSec